80C51A11

CMOS Single-Chip 8 bit Microcontroller with CAN Controller

Description

The 80C51A11 is a stand alone, high performance CMOS microcontroller designed for use in automotive and industrial applications..

The 80C51A11 retains all features of the MHS 80C51 with extended ROM capacity (16 K bytes), 256 bytes of RAM, a 7-source 2-level interrupt, a full duplex serial port, an on-chip oscillator and clock and two 16 bits timers.

In addition, the 80C51A11 has an 8-bit 8-channel A/D converter, a serial peripheral interface compatible with SPI, an advanced 5 channel Event and Waveform Controller, a CAN network line controller and a 256 bytes extra RAM . A part of this RAM is used to store the CAN messages. An optional 256 bytes E2PROM is also provided.

The CAN controller is fully compliant with the Bosch CAN standard rev 2.0 part A (part B passive). It implements all features of a full CAN controller able to handle all frames of the protocol with 14 simultaneous messages. It includes 14 identifier registers each with independent mask and uses the 256 bytes DPRAM to store the received and transmitted messages.

The fully static design of the 80C51A11 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

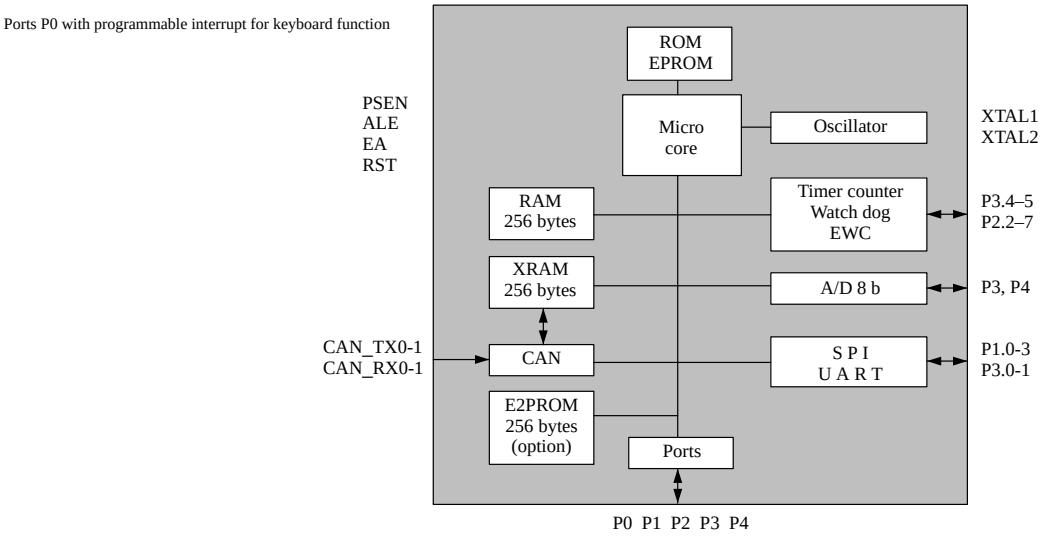
The design is optimised to ensure low EMC emission and susceptibility.

This circuit is manufactured using SCMOS process which allows to run from 0 up to 18 MHz in the automotive temperature range –40°C to +125°C.

Features

- 80C51 core architecture
- 256 bytes of RAM, 256 bytes of XRAM
- Optional 256 bytes of E2PROM
- 16 K bytes of ROM or OTP; options 8K & 32 K
- Four 8-bit I/O ports
- Two 16 bit timer/counter
- A five channels Event and Waveform Controller with:
  - input capture
  - output compare and PWM
  - High security watchdog
  - Upward compatible with PCA
- A 8-bit resolution analog to digital converter with eight multiplex inputs
- One port with programmable interrupt for keyboard function
- Several power reduction modes with enhanced wake up capabilities
- Full duplex UART compatible with standard 80C51
- A serial peripheral interface (SPI)
- Full CAN controller
  - Fully Compliant with CAN standard rev 2.0 A (2.0 B Passive)
  - 256 bytes DPRAM for received and transmitted messages (shared with XRAM)
  - 14 Identifier Registers with all bits individually maskable
  - 1 Mbit/s Maximum Transfer Rate
  - Idle and Sleep modes
  - Integrated line interface circuitry (output drivers, input comparators, Vcc/2 generator)
- PQFP 52 or PLCC 52 package

Block Diagram



Pin Configuration

Pin PQFP52	Name	Function	Pin PQFP52	Name	Function
3	ANAVSS	Analog VSS	29	P2.3/A11/EWX0	Address bus high order or EWC module 0 external I/O
4	P4.0/ANA0/VCC1/2	Analog Input 0 or VCC / 2 output	30	P2.4/A12/EWX1	Address bus high order or EWC module 1 external I/O
5	P4.1/ANA1	Analog Input 1	31	P2.5/A13/EWX2	Address bus high order or EWC module 2 external I/O
6	P4.2/ANA2	Analog Input 2	32	P2.6/A14/EWX3	Address bus high order or EWC module 3 external I/O
7	P4.3/ANA3	Analog Input 3	33	P2.7/A15/EWX4	Address bus high order or EWC module 4 external I/O
8	P4.4/ANA4	Analog Input 4	34	PSEN	Program store enable
9	P4.5/ANA5	Analog Input 5	35	ALE/PROG	Address latch enable/Program pulse
10	P4.6/ANA6/REF+	Analog Input 6 or Analog positive reference	36	EA/VPP	External access enable/Programming supply voltage
11	P4.7/ANA7/REF-	Analog Input 7 or Analog negative reference	37	P0.7/AD7/KB0.7	Mux. low order address & data bus or Keyboard
12	ANAVCC	Analog VCC	38	P0.6/AD6/KB0.6	Mux. low order address & data bus or Keyboard
13	RST	Reset	39	P0.5/AD5/KB0.5	Mux. low order address & data bus or Keyboard
14	P3.0/RXD	Serial receive port	40	P0.4/AD4/KB0.4	Mux. low order address & data bus or Keyboard
15	P3.1/TXD	Serial transmit port	41	P0.3/AD3/KB0.3	Mux. low order address & data bus or Keyboard
16	P3.2/INT0	External interrupt 0	42	P0.2/AD2/KB0.2	Mux. low order address & data bus or Keyboard
17	P3.3/INT1	External interrupt 1	43	P0.1/AD1/KB0.1	Mux. low order address & data bus or Keyboard
18	XTAL2	Crystal output	44	P0.0/AD0/KB0.0	Mux. low order address & data bus or Keyboard
19	XTAL1	Crystal input	45	VSS	
20	VCC		46	VCC	
21	VSS		47	P1.0/MISO	SPI master in ,slave out
22	P3.4/T0	Timer/counter 0 input	48	P1.1/MOSI	SPI master out, slave in
23	P3.5/T1/CAN TX1	Timer/counter 1 input	49	P1.2/SCK	SPI serial clock I/O
24	P3.6/WR	External data memory write strobe	50	P1.3/SS	SPI slave select
25	P3.7/RD	External data memory read strobe	51	P1.4/CAN_TX0	CAN TX0
26	P2.0/A08	Address bus high order	52	P1.5/CAN_TX1	CAN TX1
27	P2.1/A09	Address bus high order	1	P1.6/CAN_RX0	CAN RX0
29	P2.2/A10/ECI	Address bus high order or EWC count input	2	P1.7/CAN_RX1	CAN RX1